	Type	Hits	Search Text	DBs	Time Stamp
1	IS&R	2	(("6350649") or ("6518671")).PN.	USPAT; US-PGPUB	2003/06/26 09:26
2	IS&R	10	(("6153935") or ("4430365") or ("5208170") or ("5371047") or ("5723381") or ("5948701") or ("4549927") or ("5189506") or ("5328553") or ("5654216")).PN.	USPAT; US-PGPUB	2003/06/26 09:31
3	IS&R	39	(("5960318") or ("6004883") or ("6133144") or ("6165898") or ("6174804") or ("6181012") or ("6287961") or ("6326300") or ("6350649") or ("6358797") or ("6362093") or ("6365505") or ("6372631") or ("6372635") or ("6380078") or ("6383919") or ("6391766") or ("6399486") or ("6399496") or ("6429116") or ("6429119") or ("6429523") or ("6440838") or ("6440863") or ("6444573") or ("6518671") or ("4962058") or ("5539255") or ("5663101") or ("5960254") or ("4470874") or ("6097092") or ("6171971") or ("6221229") or ("6221229") or ("4541169") or ("4541168") or ("4600624") or ("4601939") or ("4799990")).PN.	USPAT; US-PGPUB	2003/06/26 09:32
4	BRS	8	("5635423" | "5753967" | "5795823" | "5801094" | "5814557" | "5886410" | "5920790" | "5926732").PN.	USPAT	2003/06/26 09:55
5	BRS	12	("4966870" | "5466636" | "5612254" | "5808335" | "5891799" | "5895239" | "5918120" | "6008083" | "6022776" | "6037215" | "6083824" | "6156643").PN.	USPAT	2003/06/26 09:59
6	BRS	15	("4966870" | "5466636" | "5612254" | "5808335" | "5891799" | "5895239" | "5918120" | "6022776" | "6074952" | "6083824" | "6159839" | "6265271" | "6329255" | "6339027" | "6350649").PN.	USPAT	2003/06/26 10:01
7	IS&R	1794	(257/758).CCLS.	USPAT; US-PGPUB	2003/06/26 10:44

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
1	US 6133144 A	11	Self aligned dual damascene process and structure with low parasitic capacitance	438/634	257/758; 257/760; 257/761; 257/776; 438/618; 438/622; 438/624; 438/638	Tsai, Ming-Hsing et al.
2	US 6287961 B1	19	Dual damascene patterned conductor layer formation method without etch stop layer	438/638	257/E21.579; 438/637; 438/783; 438/924	Liu, Chung-Shi et al.
3	US 6350649 B1	11	Bit line landing pad and borderless contact on bit line stud with etch stop layer and manufacturing method thereof	438/256	438/253	Jeong, Hong-Sik et al.
4	US 6399496 B1	10	Copper interconnection structure incorporating a metal seed layer	438/687	257/E21.585; 257/E23.161; 438/633; 438/658	Edelstein, Daniel Charles et al.
5	US 6440838 B1	10	Dual damascene structure employing laminated intermediate etch stop layer	438/618	438/637	Lui, Ming-Huei et al.
6	US 6440863 B1	14	Plasma etch method for forming patterned oxygen containing plasma etchable layer	438/710	438/711; 438/717; 438/723	Tsai, Chia-Shiun et al.
7	US 6444573 B1	13	Method of making a slot via filled dual damascene structure with a middle stop layer	438/638	438/624; 438/633; 438/634; 438/666; 438/668; 438/687	Wang, Fei et al.
8	US 6518671 B1	14	Bit line landing pad and borderless contact on bit line stud with localized etch stop layer and manufacturing method thereof	257/758	257/760; 438/639	Yang, Won-Suk et al.

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	Document ID	Pages	Title	Current OR	Current XRef	Inventor
1	US 20010015498 A1	12	Semiconductor device and method of fabricating the same	257/758		Miyamoto, Yasushi
2	US 20020158339 A1	61	Wiring structure of a semiconductor integrated circuit and a method of forming the wiring structure	257/758		Yamamoto, Hiroshi
3	US 20020163080 A1	71	Semiconductor device and its manufacture	257/758		Taniguchi, Toshio et al.
4	US 4933743 A	17	High performance interconnect system for an integrated circuit	257/742	257/753; 257/758; 257/763; 257/774; 257/776; 257/E23.143; 257/E23.145; 257/E23.16	Thomas, Michael E. et al.
5	US 5500558 A	28	Semiconductor device having a planarized surface	257/758	257/760; 257/E21.244; 257/E21.245	Hayashide, Yoshio
6	US 5661344 A	8	Porous dielectric material with a passivation layer for electronics applications	257/758	257/637; 257/642; 257/759; 257/760; 257/E21.273; 257/E21.576; 257/E21.577	Havemann, Robert H. et al.
7	US 5726499 A	26	Semiconductor device having a minute contact hole	257/774	257/758; 257/776; 257/E21.577; 257/E21.584; 257/E23.019	Irinoda, Mitsugu
8	US 6130449 A	32	Semiconductor memory device and a method for fabricating the same	257/296	257/306; 257/758; 257/E21.656; 257/E21.66; 257/E29.343	Matsuoka, Hideyuki et al.
9	US 6187662 B1	11	Semiconductor device with low permittivity interlayer insulating film and method of manufacturing the same	438/624	257/758; 257/760; 257/E21.576; 438/781; 438/782	Usami, Tatsuya et al.

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
10	US 6255151 B1	56	Semiconductor integrated circuit device and method of manufacturing same	438/197	257/296; 257/306; 257/307; 257/308; 257/309; 257/758; 257/E21.008; 438/238; 438/239; 438/240; 438/241; 438/253; 438/256; 438/396; 438/397; 438/398; 438/399; 438/622; 438/642; 438/688	Fukuda, Takuya et al.
11	US 6255685 B1	63	Semiconductor device and method of manufacturing the same	257/306	257/758; 257/E21.577; 257/E21.579; 257/E21.585; 257/E23.142	Kuroda, Hideaki
12	US 6300682 B1	8	High performance MIM (MIP) IC capacitor process	257/758	257/665; 257/E21.008; 438/267	Chen, Chia Hsiang
13	US 6316833 B1	9	Semiconductor device with multilayer interconnection having HSQ film with implanted fluorine and fluorine preventing liner	257/758	257/623; 257/757; 257/760; 257/E23.167; 438/694; 438/697; 438/780	Oda, Noriaki
14	US 6362528 B1	31	Semiconductor device and method of manufacturing the same	257/758	257/784; 257/E23.02	Anand, Minakshisundaran Balasubramanian
15	US 6384482 B1	5	Method for forming a dielectric layer in a semiconductor device by using etch stop layers	257/758	257/760; 438/624; 438/633; 438/634	Yang, Chih-Sheng et al.

22	US 6501127 B2	16	Semiconductor device including a nonvolatile memory-cell array, and method of manufacturing the same	257/321	257/316; 257/758; 257/E21.683; 257/E27.081	Mori, Seiichi
23	US 6509649 B1	5	Semiconductor device and fabricating method thereof	257/758	257/767	Sugai, Kazumi
24	US 6524944 B1	8	Low k ILD process by removable ILD	438/623	257/642; 257/758; 257/759; 257/760; 438/421; 438/422; 438/634; 438/778	Rangarajan, Bharath et al.
25	US 6531779 B1	15	Multi-layer interconnection structure in semiconductor device and method for fabricating same	257/758	257/354; 257/401; 257/409	Oda, Noriaki
26	US 6531783 B1	7	Method of via formation for multilevel interconnect integrated circuits	257/774	257/734; 257/758; 257/759; 257/760; 257/773	Kalnitsky, Alexander

	Document ID	Pages	Title	Current OR	Current XRef	Inventor
27	US 6541862 B2	28	Semiconductor device including a plurality of interconnection layers, manufacturing method thereof and method of designing semiconductor circuit used in the manufacturing method	257/751	257/758; 257/773	Amishiro, Hiroyuki et al.